AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of forming a gate in a semiconductor device, comprising ~~the steps of:~~

forming a gate pattern on which a gate oxide film and a conductive layer are stacked at a give region on a semiconductor substrate~~; and~~

forming a hard mask on top of the gate pattern; and

performing oxygen plasma treatment to form oxide films~~ at the~~ sides of the conductive layer and not on the hard mask.

2. (Original) The method as claimed in claim 1, wherein the gate oxide film is formed using a silicon oxide film or a high-dielectric metal oxide film.

3. (Currently Amended) The method as claimed in claim 2, wherein the silicon oxide film include SiO_2 and ~~SiOxNy~~ SiO_xN_y.

4. (Original) The method as claimed in claim 2, wherein the high-dielectric metal oxide film includes HfO_2, ZrO_2, Hf-Al-O, Zr-Al-O, Hf-silicate and Zr-silicate.

5. (Original) The method as claimed in claim 1, wherein the conductive layer has a structure on which a polysilicon film, an anti-diffusion film, a metal film and a hard mask are stacked.

6. (Original) The method as claimed in claim 1, wherein the conductive layer has a structure on which an anti-diffusion film, the conductive layer and the hard mask are stacked.

7. (Currently Amended) The method as claimed in claim 5, wherein the anti-diffusion film is formed using any one of $WN\sout{x}_{\underline{x}}$, a stack film of W and $WN\sout{x}_{\underline{x}}$, a stack film of ~~Wsix~~ $\underline{WSi_x}$ and $WN\sout{x}_{\underline{x}}$, $TaSi\sout{x}_{\underline{x}}N\sout{y}_{\underline{y}}$ and $TiAl\sout{x}_{\underline{x}}N\sout{y}_{\underline{y}}$.

8. (Currently Amended) The method as claimed in claim 6, wherein the anti-diffusion film is formed using any one of $WN\sout{x}_{\underline{x}}$, a stack film of W and $WN\sout{x}_{\underline{x}}$, a stack film of ~~Wsix~~ $\underline{WSi_x}$ and $WN\sout{x}_{\underline{x}}$, $TaSi\sout{x}_{\underline{x}}N\sout{y}_{\underline{y}}$ and $TiAl\sout{x}_{\underline{x}}N\sout{y}_{\underline{y}}$.

9. (Original) The method as claimed in claim 5, wherein the metal film is formed using any one of W, Ta, TaN, Ti and TiN.

10. (Original) The method as claimed in claim 6, wherein the metal film is formed using any one of W, Ta, TaN, Ti and TiN.

11. (Original) The method as claimed in claim 1, wherein the oxygen plasma treatment is implemented by applying the RF source power of 100 ~ 3000W and the RF bias power of 0 ~ 100W.

12. (Original) The method as claimed in claim 1, wherein the oxygen plasma treatment is performed using a gas containing oxygen such as O_2, O_3, N_2O, NO or H_2O, or a mixture of them.

13. (Original) The method as claimed in claim 1, wherein the oxygen plasma treatment is performed using oxygen and hydrogen together.

14. (Original) The method as claimed in claim 11, wherein the flow ratio of oxygen/hydrogen is 0.01 ~ 0.2.

15. (Original) The method as claimed in claim 1, wherein the oxygen plasma treatment is implemented in a state where the substrate temperature is 0 ~ 450°C.

16. (Original) The method as claimed in claim 1, further comprising the step of implementing the oxygen plasma treatment by illuminating ultraviolet rays on the top of the substrate.

17. (Original) The method as claimed in claim 1, further comprising the step of performing an annealing process after the oxygen plasma treatment is performed.

18. (Currently Amended) The method as claimed in claim ~~15~~ 17, wherein the annealing process is performed at a temperature of 600 ~ 1000°C for 10 seconds ~ 60 minutes ~~at~~ in a nitrogen, hydrogen, argon or vacuum atmosphere.

19. (Currently Amended) A method of forming a gate in a semiconductor device, comprising the steps of:

forming a gate pattern on which a gate oxide film, a polysilicon film, an anti-diffusion film, and a metal film ~~and a hard mask~~ are stacked at a given region on a semiconductor substrate;

forming a hard mask on the gate pattern;

performing oxygen plasma treatment to form oxide films ~~at the~~ only on sides of the gate pattern and not on the hard mask; and

performing an annealing process for improving the film quality of the oxide film.

20. (Currently Amended) A method of forming a gate in a semiconductor device, comprising the steps of:

forming a gate pattern on which a gate oxide film, an anti-diffusion film, and a metal film ~~and a hard mask~~ are stacked at a given region on a semiconductor substrate;

forming a hard mask on the gate pattern;

performing oxygen plasma treatment to form oxide films ~~at the~~ only on sides of the gate pattern and not on the hard mask; and

performing an annealing process for improving the film quality of the oxide film.